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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,802	12/22/2000	Michihide Kimura	1448.1007	9060

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EXAMINER

PAN, DANIEL H

ART UNIT	PAPER NUMBER.
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2183

DATE MAILED: 03/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/741,802

Applicant(s)

KIMURA ET AL.

Examiner

pan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 December 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 24-28 is/are allowed.
- 6) ☐ Claim(s) 1-16, 18, 19, 23, 29 and 30 is/are rejected.
- 7) ☒ Claim(s) 17 and 20-22 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 December 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 1,2.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

1. Claims 1-30 are presented for examination.

Claim 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claim 1, the meaning of "not prescribed a functional specification" is not clear. It is not sure whether the language is directed to the functional operation of the instruction, or a specific operand designation, or the format. Applicant is welcome to clarify this language in the next response.

Claim 5 recites the limitation "the same instructions" in line 15. There is insufficient antecedent basis for this limitation in the claim. Suggestion : is it referring to the instruction in line 13, or any following instruction(s) of the given sequence ? Applicant is kindly suggested to provide clarification in the next response. See also "the same succeeding instructions" in line 16 for the same problem.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

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2. Claims 1-5, 7,8,10,11,12,14-16,30 are rejected under 35 U.S.C. 102(e) as being anticipated by Hartnett et al. (6,167,479) .

3. As to claim 1, Hartnett disclosed a processing apparatus (see fig.6) as claimed comprising at least :

a) a control unit [micorcontroller 178] for processing an operation instruction (see e.g. the expanded-cycle instruction) as a specific application-purpose operation (e.g. see the microcode controller controlling the instruction execution in col.9, lines 1-23, see also col.7, lines 39-55, col.8, lines 1-13 for the microcode controller during the extended cycles);

b) a specific application-purpose instruction operating unit (e.g. fig.6 [12] IP, see also fig.6) for supporting a flexible pipeline structure (see the pipeline processing in col.8, lines 27-43) and capable of being designed to carry out an operation (e.g. address generation) of the specific application-purpose instruction for each application field [subsection] (see the address generation for the corresponding subsection in col.8, lines 27-40, see col.6, lines 59-67 for background, the extended cycle instruction added more delays cycles, see col.7. lines 56-66).

As to the language of "not prescribe a functional specification", it is not sure what it menat as set forth in the "112" above. IN addition, Every instruction has to have a function prescribed by an opcode. Is applicat trying to say that the instrucion has no opcode ? For examination, it is assumed that this is directed to be a any instruction general in format , not having any specific form. Applicant is kindly suggested to clarify this language in the next response.

4. As to claim 2, the specific application-purpose instruction unit of Hartnett was an IP we well (see fig.1 [12 IP]).

5. As to claim 3, Hartnett's control unit [microcode controller] and the specific application-purpose instruction unit were within the core processor (e.g. see fig.6 [12], see also fig.1 [12], col.6, lines 3-13 for the IP unit for executing and control the instructions).

6. As to claim 4, Hartnett also prescribed a number of cycles (see the 2y , 1x and E cycles) when the instruction was issued to when the result was provided (see the number of cycles from the reading of the memory to the execution cycle 2x in col.6, lines 59-67, col.7, lines 56-67). Hartnett did not explicitly show the writable register for prescribing the number of cycle. No hardware was shown to store the number of cycles. However, Hartnett clearly taught the prescribing the number of cycles (see citation above), therefore , Hartnett must have a writable register, or a storage for purpose of tracking the number of cycles extended. The number of cycles was not fixed because more extended cycles could occur (col.7, lines 65-67). Therefore, the register or the storage must be writable to keep track of the number of cycles.

7. As to the "result" provided in the claim , Hartnett 's result must be provided before the start of 2x cycle, otherwise the number of cycles would have been extended continually.

8. As to claim 5, due to the problem set forth in the "112" above, the claim language "the same instructions" is assumed to be any instructions in the subsequent

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stages. With this interpretation, Hartnett also prescribed the number of cycle from when the issue of an instruction (the first instruction in the interrupt handler) to when the same instructions were issued (see the fetch of the original instruction at $MX+x+1$ cycle after the fetch of the first instruction in col.16, lines 1-2, col.17, lines 1-16).

Applicant is welcome to provide feedback or correction to more clearly define the scope.

9. As to claims 7,11, Hartnett also disclosed

a) a saving of the context after the execution interrupted (e.g. see col.11, lines 5-37);

b) confirmation unit to confirm whether or not the operation exception had detected during the specific application purpose operation instruction (e.g. see the interrupt type in col.10, lines 51-53, see also the state reflecting the fault and non-fault type interrupt in col.11, lines 5-37, see also determination of what caused the interrupt in col.12, lines 5-8, the specific application – purpose instruction was already taught in 7, lines 41-65);

c) exception n processing unit which carried out exception processing when the exception was detected (e.g. see the interrupt handler in col.12, lines 5-51);

d) return unit returning from interrupt (e.g. see col.12, lines 10-51, see 17, lines 27-40, see also the return instruction in col.15, lines 44-56, col.17, lines 1-40).

10. As to claims 8, 12, Hartnett also included a second confirmation unit (see the interrupt testing in col.19, lines 4-17) to confirm whether or not operation state had been set to exception during the execution (see the injection bits in col.19, lines 18-37).

11. As to claims 10,14, Hartnett also included a memory 354 which stored values (injection bits) to indicates detection of the interrupt exception during the execution (e.g. see col.19, lines 4-23, col.20, lines 35-47, col.21, lines 24-35).

12. As to claim 15, Hartnett also confirmed the state of the operation state (e.g. see the injection bit in the memory in col.19, lines 18-27, col.21, lines 28-42).

13. As to claim 16, Hartnett also confirmed the instruction for settings state detected (e.g. see corresponding instruction set by the state in col.19, lines 4-23).

14. As to claim 30, Hartnett also included at least :

a) detection unit for detecting an operation exception during execution of specific application-purpose instruction (e.g. see col.9, lines 34-59);

b) an execution interrupt unit for temporarily stopping the execution of the computer program (see the suspension of the instruction execution in col.9, lines 34-59, see also the redirect of the program flow into the exception handler in col.4, lines 40-47 for background teaching);

c) saving the context when the detection occurred (e.g. see the saved state in col.11, lines 5-37);

d) an exception processing unit which performed an exception processing (see the interrupt handler in col.11, lines 55-67, col.12, lines 1-51);

e) restarted the execution after the exception processing (e.g. see the re-started execution in col.12, lines 10-51, see also the resume of the execution in col.4, lines 60-65 for background teaching).

15. As to the specific application purpose instruction, Hartnett's standard and non-standard instructions are applicable as specific application purpose instructions because they were directed to the program executed in a simulation system (e.g. see col.1, lines 14-26). Simulation is a specific application.

16. Claims 9, 13, 18, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartnett et al. (6,167,479) in view of Swoboda et al. (6,553,513).

17.

18. Limitations of the parent claims 1, 7 have been discussed in previous paragraph, therefore, it will not be repeated herein.

19. As to claims 9,13,18, Hartnett did not specifically show the confirmation of the instruction for breaking (or the break point) as claimed. However, Swoboda disclosed an instruction for breaking [breakpoint] (e.g. see col.8, lines 20-23). It would have been obvious to one of ordinary skill in the art to use Swoboda in Hartnett for including instruction for breaking as claimed because the use of fndjf could provide Hartnett the control ability of the exception handler to adapt to different type of the exception

condition, thereby expanding the processing capability of Hartnett in a given system, and it could be readily achieved by defining the break instruction of Swoboda into Hartnett's exception handler with modified configuration parameters, such as the instruction type, and length, so that the break instruction of Swoboda could be recognized by Hartnett, and because Hartnett also taught that the interrupt injection bit was applicable to a block of instructions rather than a respective instruction (e.g. see col.20, lines 5-8), which was a suggestion of the need of using an interrupt instruction, such as a breakpoint, into a specific segment of the instruction sequence being tested, and for the above reasons, provided a motivation.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

20. Claim 19, 23, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over f Hartnett (6,167,479) in view of Swoboda (6,553,513).

21. As to claims 19, 29, Hartnett disclosed at least :

a) operation exception detection flag which indicated operation exception (e.g. see the entry point in injected bit set to 1 in fig.11);

b) specific application purpose operation instruction unit [410] which set a valid state when the exception has detected during the execution of the specific application instruction (e.g. see col.20, lines 28-47);

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c) a flag control unit [414]-[420] for notifying to interrupt control unit [421] that an interrupt due to an operation exception of the specific application instruction was to be generated when the state was valid (e.g. see col.20, lines 28-47);

the interrupt control unit carried out control relating to the generation of the interrupt (see col.20, lines 44-47).

Hartnett's instructions were specific application instructions because it was directed to simulation application (e.g. see col.1, lines 13-27).

22. Hartnett did not specifically show his valid state was set during the execution of a trap as claimed. Hartnett did not show the trap instruction. However, Swoboda disclosed a trap instruction (col.25, lines 1-20). It would have been obvious to one of ordinary skill in the art to use Swoboda in Hartnett for including the trap instruction as claimed because the use of Swoboda could enhance the processing capability of Hartnett's exception handler to accept specific type of the interrupt, such as the trap, and it could be readily done by configuring the trap instruction of Swoboda into Hartnett such that the trap instruction could be recognized by Hartnett, and because one of ordinary skill in the art should be able to recognize that the type of the exceptions, such as the address reference violation (col.10, lines 5-10), would involve the illegal reference at specific location, which would have caused the infinite loop in the instruction processing, and therefore suggested the need of the detection of the possible trap instruction, and in doing so, provided a motivation.

23. As to claim 23, Hartnett did not show his system was used for imaging processing as claimed. However, claim 23 does not recite any specific feature or structure of the imaging processing. Therefore, the examiner believes that a language just reciting an instruction for "image processing" does not have a patentable weight. Nevertheless, Hartnett taught that his system was a digital processing system and could be used for various architectures (e.g. see col.5, lines 65-67, col.6, lines 1-3), therefore, one of ordinary skill in the art should be able to recognize other architectures, such as the digital signal processing system could be used for imaging processing.

24. Claim 6 is would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

25. Claims 17 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record teaches further the combined features of the indication of the instruction address that has interrupted the program is for detecting an operation exception that occurred during the execution of the instruction can be detected and the confirmation of the operation exception is detected or not.

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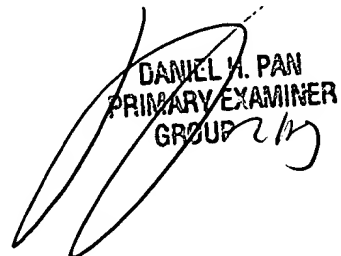
26. Claims 20,21,22, objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art or record further teaches the exception detection flag invalidating instruction, the exception detection flag read instruction , and the exception detection flag write instruction , respectively for each claim.

27. Claims 24-28 are allowable over the art of record for reciting the combined features of the condition code register and the branch/interrupt return instruction control unit for determining the interrupt generation based on the value held in the condition code register and the value in the instruction field during the execution of the trap instruction, and the notification that the interrupt is to be generated.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


DANIEL H. PAN
PRIMARY EXAMINER
GROUP 1

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